Listing of Claims

Claim 1 (Canceled)

Claim 2 (Currently Amended): A high resolution potentiometer comprising:

a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable to be set to offer a second resistance, wherein said first resistance is not equal to said second resistance; and

a controller block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance.

Claim 3 (Canceled)

Claim 4 (Currently Amended): The high resolution potentiometer of claim 2 ~~3~~, wherein said controller block receives a desired resistance value and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said high resolution potentiometer at least substantially equals said desired resistance.

Claim 5 (Currently Amended): The high resolution potentiometer of claim 2 ~~3~~, wherein said controller block receives values corresponding to said first resistance and said second resistance, and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said high resolution potentiometer at least substantially equals a desired resistance.

Claim 6 (Currently Amended): The high resolution potentiometer of claim 2 ~~3~~, further comprising a resistor connected in series with said first digital potentiometer and said second digital potentiometer connected in parallel.

Claim 7 (Previously Amended): A high resolution potentiometer comprising:

a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable to be set to offer a second resistance, wherein said first resistance is not equal to said second resistance; and

a controller block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance.

wherein said first potentiometer, said second potentiometer and said controller block are implemented in a single integrated circuit.

Claim 8 (Currently Amended): A system comprising:

a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable to be set to offer a second resistance, wherein said first resistance is not equal to said second resistance; and

a controller block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance.

Claim 9 (Canceled):

Claim 10 (Currently Amended): The system of claim 8 9, wherein said controller block receives a desired resistance value from ~~said~~ a processor and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said system at least substantially equals said desired resistance.

Claim 11 (Currently Amended): The system of claim 8 9, wherein said controller block receives values corresponding to said first resistance and said second resistance from ~~said~~ a processor, and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective

resistance provided by said first digital potentiometer and said second digital potentiometer are connected in parallel at least substantially equals a desired resistance.

Claim 12 (Currently Amended): The system of claim ~~8~~ 9, further comprising a resistor connected in series with said first digital potentiometer and said second digital potentiometer connected in parallel.

Claim 13 (Previously Amended): A system comprising:

a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable to be set to offer a second resistance,whereinsaid first resistance is not equal to said second resistance;

a controller block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance; and

wherein said first potentiometer, said second potentiometer and said controller block are implemented in the form of a single integrated circuit.

Claim 14 (Original): The system of claim 13, further comprising a processor, wherein said controller block receives a desired resistance value from said processor and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said system at least substantially equals said desired resistance.